

Appl. No.: 09/735,266
Amdt. dated: September 2, 2003
Reply to Office Action of June 2, 2003

Patent
Docket No.: 253/300
19535-7140

REMARKS

An IDS filed on December 11, 2000 has not yet been considered. Applicants request this IDS be considered.

Claims 1-3, 6-13, and 15-29 stand rejected based on U.S. Patent No. 5,557,764 issued to Stewart et al. ("Stewart"). Claims 4 and 5 stand rejected under 35 U.S.C. 103 based on Stewart in view of U.S. Patent No. 6,154,837 issued to Fudeyasu et al. ("Fudeyasu"). Claims 1 and 24 have been amended. New claims 30-35 have been added.

Stewart discloses:

An apparatus is provided for processing a plurality of interrupts in a processor system, comprising a plurality of interrupt vector registers each having an interrupt trigger input, each of the interrupt vector registers containing a programmable interrupt vector. A multiplexer is connected to the interrupt vector registers and control logic controls the multiplexer to select one of the interrupt vectors as the selected interrupt vector upon activation of the corresponding interrupt trigger. A slot memory address counter receives the selected interrupt vector through the multiplexer, the slot memory address being controlled by the control logic to load the selected interrupt vector.

(Col. 2, lines 5-17).

Stewart clearly discloses that "A slot memory address counter receives the selected interrupt vector through the multiplexer, the slot memory address being controlled by the control logic to load the selected interrupt vector."

In contrast, claim 1 as amended recites "an interrupt vector from said interrupt store to be loaded directly into an execution unit of the processor," which is neither disclosed nor suggested by Stewart. Therefore, applicant submits that claim 1 as amended is patentable over Stewart.

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Given that claims 2-19 depend from claim as amended, applicant submits that these claims are also patentable over Stewart.

Claim 20 recites "delivering a pre-stored interrupt vector directly to the execution unit of the processor," which is neither disclosed nor suggested by Stewart. Therefore, applicant submits that claim 20 is patentable over Stewart. Given that claims 21-23 depend from claim 20, applicant submits that these claims are also patentable over Stewart.

Stewart discloses:

Each SSP contains eight vector registers 10. The vector registers 10 contain start addresses of sequences.

(Col. 3, lines 35-36).

Claim 24 as amended recites "causing the processor... to receive an interrupt vector comprising a branch instruction op-code and address," which is neither disclosed nor suggested by Stewart. Therefore, applicant submits that claim 24 as amended is patentable over Stewart. Given that claims 25-29 depend from claim 24 as amended, applicant submits that these claims are also patentable over Stewart.

Claims 4 and 5 stand rejected under 35 U.S.C. 103 based on Stewart in view of Fudeyasu. Claim 1 as amended recites "an interrupt vector from said interrupt store to be loaded directly into an execution unit of the processor. Stewart and Fudeyasu, either alone or in combination, neither teach nor suggest this element of claim 1 as amended. Therefore, applicant submits that claim 1 as amended is patentable over Stewart in view of Fudeyasu. Given that claims 4 and 5 depend from amended claim 1, applicants submit that these claims are also patentable over Stewart in view of Fudeyasu.

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CONCLUSION

Allowance of the claims is respectfully requested. The Examiner may call the Assignee's attorney at (650) 849-4422 to further advance prosecution of this case to issuance.

If the Commissioner determines that additional fees are due or that an excess fee has been paid, the Patent Office is authorized to debit or credit (respectively) Deposit Account No.

50-2518, referencing billing no. 7010642001.

DATE: September 2, 2003

Respectfully submitted,

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